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10/567,070	02/03/2006	Michiel Jos Van Duuren	NL03 0977 US1	9477

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EXAMINER	
LAPPAS, JASON	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/567,070	VAN DUUREN, MICHIEL JOS	
	Examiner	Art Unit	
	JASON LAPPAS	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/20/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment dated 11/20/2007 in which claims 1 and 5 were amended, and claim 15 was added has been entered of record. Currently, claims 1-15 are pending in light of the amendment.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-2, 5-6, 14-15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiga (U.S. Patent 6,778,443), in view of Torii (U.S. Patent 7,092,297).

Claim 1. Shiga teaches a method for operating an array of non-volatile (Shiga, Title) charge trapping memory devices (Shiga teaches flash memory cells which are charge trapping memory devices), comprising:

before block erasing the array by discharging substantially all of the non-volatile charge trapping memory devices of the array, block programming the array by charging substantially all (after ease execution is confirmed the first block is pre-programmed, by charging, and subsequently undergoes data erase, steps repeat for proceeding blocks.

Shiga Col 1 lines 33-34. When all blocks are selected all blocks are preprogrammed then erased. Examiner would like to point out that substantially all is not exactly all.) of the non-volatile charge trapping memory devices of the array (Nonvolatile Shiga, Title).

It is noted that Shiga is silent with respect to by programming by charging and erasing by discharging. Torii teaches a flash ONO charge trapping memory device that charges during programming (injecting electrons in nitride region, Torii Col 1 lines 36-39) and discharges during erasing (injecting holes in the nitride region, Torii Col 1 lines 36-39), for the purpose of dual bit programming (Torii Col 1 Lines 33-35). An ONO memory cell is a suitable replacement for a floating gate memory cell.

The selection of something based on its known suitability for its intended use has been held to support a *prima facie* case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.,* 325 U.S. 327, 65 USPQ 297 (1945).

Since Shiga and Torii are both from the same field of endeavor (flash memory), the purpose disclosed by Torii would have been recognized in the pertinent art of Shiga.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use an ONO cell as taught by Torii in place of the floating gate cells taught by Shiga for the purposes of dual bit programming.

Claim 2. Shiga and Torii teach a method according to claim 1, furthermore comprising after the erase operation, programming some of the non-volatile memory devices of the array (after erase execution is confirmed, the first block is preprogrammed, Shiga Col 1 lines 33-35), depending on data content to be stored in the non-volatile memory devices of the array (erase is undergone only to blocks that need it, Shiga Col 1 43-46).

Claim 5. Shiga teaches an electrical device comprising an array of non-volatile charge trapping memory devices (Shiga, Title), comprising: means for block programming the array by charging (addressed in 103 combination of claim 1 using ONO taught by Torii) substantially all of the non-volatile charge trapping memory devices of the array (after ease execution is confirmed the first block is pre-programmed and subsequently undergoes data erase, steps repeat for proceeding blocks. Shiga Col 1 lines 33-34. When all blocks are selected all blocks are preprogrammed then erased.), means for block erasing the array by discharging (addressed in 103 combination of claim 1 using ONO taught by Torii) substantially all of the programmed non-volatile charge trapping memory devices of the array (erase occurs after preprogram Col 1 lines 32-34), control means for controlling the array of non-volatile charge trapping memory devices such that before block erasing of substantially all of the non-volatile memory devices of the array, substantially all of the non-volatile memory devices of the array are block programmed (means for controlling the array for preprogramming is the process check Col 1 lines 43-47).

Claim 6. An electrical device according to claim 5, wherein the non-volatile memory device comprises a transistor having a channel and a control gate (Torii Fig 2A), a dielectric charge trapping layer being located between the channel and the control gate (Torii Fig 2A teaches ONO, which contains nitride as dielectric charge trapping area.).

Claim 14. An electrical device according to claim 5, wherein the array of non-volatile memory devices forms a non-volatile memory (this is an inherent structure of a non-volatile memory array).

Claim 15. A method according to claim 1, wherein the non-volatile memory devices of the array each include a dielectric charge trapping layer (nitride region of ONO taught by Torii as addressed in claim 1) and wherein block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array includes trapping charge in the dielectric charge trapping layers (nitride regions of ONOs taught by Torii are the dielectric charge trapping layers).

2. Claim 3-4 rejected under 35 U.S.C. 103(a) as being unpatentable over Shiga (U.S. Patent 6,778,443), in view of Torii (U.S. Patent 7,092,297), further in view of Yamazoe (U.S. Patent 7,009,890).

Claim 3. Shiga teaches a method according to claim 2, furthermore comprising reading the data content stored in a non-volatile memory device of the array (reading verification Col 9 lines 7-10). Dielectric charge trapping layer is nitride region of ONO taught by Torii as addressed in claim 1.

It is noted that Shiga and Torii are silent with respect for reading the data content stored in a non-volatile memory device of the array at least one further non-volatile memory device having a dielectric charge trapping layer is used as reference cell which

is programmed and erased for a block programming and block erase, respectively, of the non-volatile memory devices in the array.

However Yamazoe teaches reference memory allocated in a unit of a block to be erased or programming to control the timing for a plurality of memories using information from the reference cell (Yamazoe Col 7 lines 3-6). Read timing is based on the deterioration of the reference memory (Col 7 lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the reference cells taught be Yamazoe in the circuit taught be Shiga and Torii to control the timing of a plurality of memories based on the deterioration of the reference cell.

Claim 4. Method according to claim 3, wherein the memory devices of the array together function as reference cells (Yamazoe teaches reference cells in the memory array since they are coupled to the same bitline decoder and are part of the same block. These are normal cells, memory devices, which function as reference cells, Yamazoe Fig 8).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiga (U.S. Patent 6,778,443) and Torii (U.S. Patent 7,092,297), further in view of Hirakawa (U.S. Patent 2001/0007541)

Claim 7. Shiga and Torii teach an electrical device according to claim 5.

It is noted that Shiga and Torii are silent with respect to the array being provided with at least one non-volatile memory device for use as a reference cell in a sense amplifier.

However Hirakawa teaches a reference cell in a sense amp. The reference cell may be part of the array or separate from the array (applicants spec page 5 lines 29-33). Having the reference cell the sense amp as opposed to the memory array is merely a rearrangement of parts.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the reference cell in the sense amp since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70

4. Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiga (U.S. Patent 6,778,443) and Torii, in view of Hirakawa (U.S. Patent 2001/0007541) further in view of Yamazoe (U.S. Patent 7,009,890).

Claim 8. Shiga, Torii and Hirakawa teach an electrical device according to claim 7.

It is noted that they are silent with respect to the array comprising means for programming and erasing the reference cell for a block-programming and block-erasing respectively of the non-volatile memory devices in the array.

However Yamazoe teaches reference memory allocated in a unit of a block to be erased or programming to control the timing for a plurality of memories using

information from the reference cell (Yamazoe Col 7 lines 3-6). Read timing is based on the deterioration of the reference memory (Col 7 lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the reference cells taught be Yamazoe in the circuit taught by Shiga and Torii to control the timing of a plurality of memories based on the deterioration of the reference cell.

Claim 9. An electrical device according to claim 7, wherein the at least one reference cell is separate from the array (claim 7 addresses a reference cell in a sense amp which is separate from the array).

Claim 10. An electrical device according to claim 7, wherein the memory devices of the array together function as reference cells (reference cells found in the memory block, Shiga Fig 8).

Claim 11. An electrical device according to claim 7, comprising means for comparing a read current from a non-volatile memory device in the array with a read current from the reference cell (reading method using a sense amplifier, Yamazoe Col 5 lines 44-49. reference cells are addressed to be found in array. Use of a reference cell in a sense amp outside the array is addressed above in claim 7).

Claim 12. An electrical device according to claim 7, comprising means for adapting a read current for reading the non-volatile memory devices in the array (the sense amplifier is a mean for adapting current for reading, addressed in claim 11, Yamazoe Col 5 lines 44-49. Adapting a current when sense amp is reading is an inherent property of a sense amp) to the aging of the reference cell (reading time is based on deterioration of the reference memory, Yamazoe Col 7 lines 11-13).

Claim 13. An electrical device according to claim 7, comprising means for adapting a required control gate voltage (sense amp outputs a wait signal, which controls the read timing depending on the degree of deterioration on the memory, Yamazoe Col 7 lines 21-27, 34-36) for reading the non-volatile memory devices in the array (adapting a read current is addressed in claim 12. Voltage is inherently adapted when current is), depending on the aging of the reference cell (time is based on deterioration of the reference memory, Col 7 lines 11-13).

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Newly amended claims 1 and 5 containing charging and discharging are addressed in 103 above using Torii. Charge trapping layer is addressed as nitride region of ONO in 103 above. Newly added claim 15 is also address in 103 above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Lappas whose telephone number is (571) 270-1272. The examiner can normally be reached on M-F 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. L./

Examiner, Art Unit 2827

/AMIR ZARABIAN/

Supervisory Patent Examiner, Art Unit 2827